

# MMIC-COMPATIBLE TERMINAL PROTECTION DEVICE

Roger Kaul  
Army Research Laboratory  
Adelphi, MD 20783

John McAdoo, W. Michael Bollen, and  
William Catoe  
Mission Research Corp.  
Newington, VA 22122

## ABSTRACT

A low-cost terminal protection device (TPD) employing only five components has been demonstrated that is compatible with monolithic microwave integrated circuits (MMICs) and suitable for phased-array applications. Using a standard low-noise, depletion-mode MESFET (metal semiconductor field-effect transistor) across a 50- $\Omega$  line, the TPD achieves a small-signal insertion loss less than 1 dB up to 3 GHz. With a single stage, the TPD attenuated 20-W pulses by 14 dB and 500-W pulses by 23 dB. Spike leakage was less than 0.1  $\mu$ J.

## INTRODUCTION

The terminal protection device (TPD) described here is designed to protect the front-end monolithic microwave integrated circuits (MMICs) of a phased-array radar from burnout by an intense, in-band microwave pulse. This pulse might be caused by the radar's internal transmitter power being reflected back into the radar receiver, or by an external high-power microwave source capable of destroying the radar's low-noise, front-end circuitry. In addition to its function as a power limiter, the TPD can be used as a switch to prevent receiver overload during the transmit period. Further, because it uses the same low-noise, metal-semiconductor field-effect transistor (MESFET) technology used in the fabrication of the front-end circuits, the TPD adds little cost to the system.

## THE CIRCUIT

The originality of this TPD lies in its simplicity: it uses only five components, which are standard parts in the MMIC design process. The broadband circuit is shown in figure 1. Typical values for the resistors are 1 k $\Omega$ , and for the capacitors, 5 pF. For narrowband operation, a tuning capability can be added to cancel the MESFET's capacitive reactance across the 50- $\Omega$  transmission line. When negative bias is applied, the MESFET gate pinches off the active channel, and the input signal passes along the 50- $\Omega$  transmission line with little attenuation. When the bias is off (0 V), the depletion-mode TPD protects the receiver circuits because the FET presents a low impedance across the line. In a phased-array application, this TPD will protect the front-end components when the array is unpowered during transport or storage.

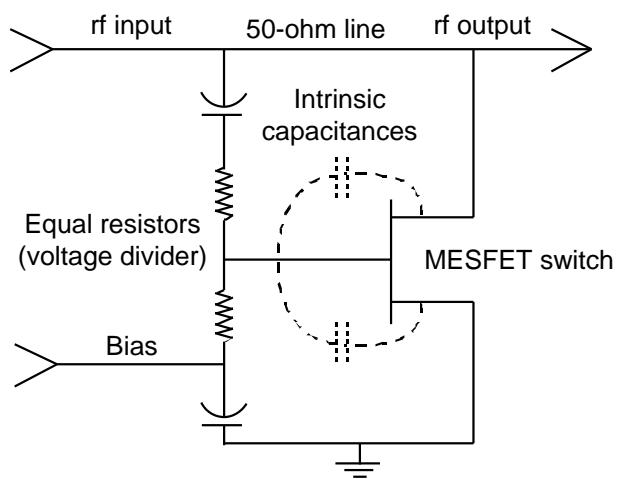


Figure 1. Broadband circuit for MMIC-compatible TPD.

## PERFORMANCE

We evaluated the quantitative performance of this device using the process control monitor chips from a 0.5- $\mu$ m, low-noise, depletion-mode, commercial foundry process. These chips were conductively epoxied to a coplanar waveguide carrier, wire-bonded, and tested in a Design Technique International test fixture. Figure 2 shows the scattering parameters  $S_{21}$  and  $S_{11}$  for a 1.3-mm-width TPD measured up to 5 GHz. The insertion loss is less than 1 dB through 3 GHz when the FET is back-biased at 1.5 V and 5.3  $\mu$ A at room temperature. The measured output third-order intercept at this bias is 25 dBm. This same device was subjected to more than 3 million 2.8-W, 1-ms-long pulses at a low duty cycle of 10 pulses per second (to avoid heating) and showed no degradation. Degradation was measured by changes noted in  $S_{21}$ ,  $S_{11}$ , and the reverse-biased, current-voltage gate characteristics. The power-handling performance of the TPD can be increased with a larger FET width, at the expense of higher capacitance across the transmission line. For low insertion loss to be maintained, this drain-source capacitance would need to be tuned out; thus, the bandwidth of the TPD would be reduced. We did not tune the TPD be-

cause we wanted to measure and understand the performance of the simplest circuit.

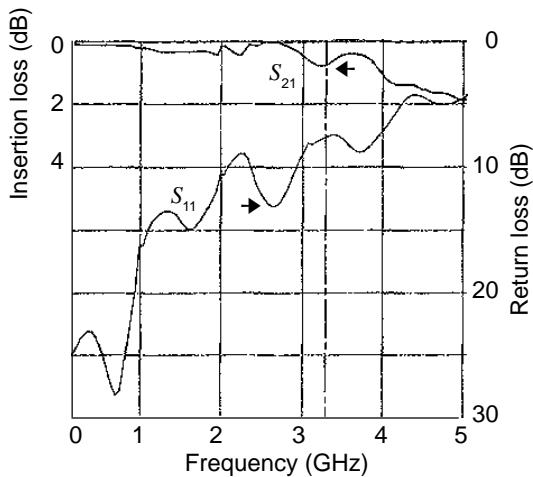
We also measured other TPDs with 100-ns-long pulse widths to determine the 0.5- $\mu$ m, low-noise FET gate width required for protection against intense microwave pulses. The minimum gate widths required for three power levels are given in table 1. These values depend on the specific MESFET fabrication process.

For these intense, short pulses, the FET avalanches, as revealed by the optical radiation present during the pulse. The high-impedance circuit connected to the FET's gate prevents it from being degraded. The source and drain junctions will degrade after many hundreds of pulses, but this intense environment is not expected for a phased-array radar.

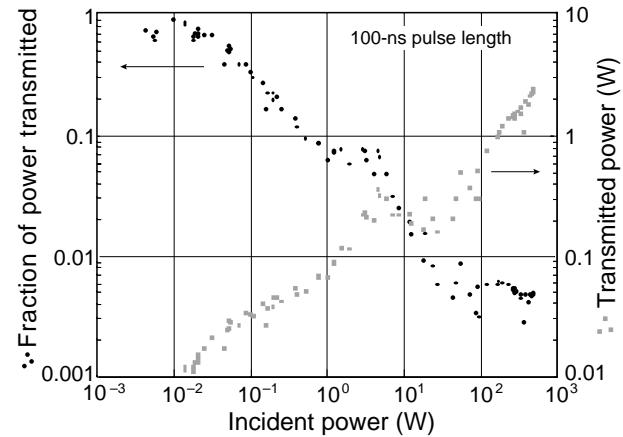
Figure 3 shows the performance of the 300- $\mu$ m gate-width TPD for incident pulses up to 500 W with a gate bias of -1.5 V. The TPD begins to limit at an incident power of 10 mW (1 V peak

**Table 1. Minimum gate width to protect against 100-ns-long pulses with incident powers listed.**

Incident power (W) at 3.3 GHz	Gate width (mm)
10	0.7
100	1.3
1000	1.7



**Figure 2. Small-signal scattering parameters for MMIC-compatible TPD.**



**Figure 3. Power transfer characteristics for MMIC-compatible TPD.**

in a  $50\text{-}\Omega$  system). For pulses over 100 W (100 V peak incident), the TPD provides over 20 dB of isolation. Since the MESFET responds to each half-cycle of the intense incident signal, no spike leakage was observed. Because the incident voltage is symmetrical with respect to ground, we used MESFETs with equal source-gate and gate-drain spacing. Therefore, the location of the source and drain changes with each half-cycle of the incident voltage.

At 500-W incident power with a 200-ns pulse length, the incident energy is 100  $\mu\text{J}$ . By measuring the transmitted power (2.5 W) and the reflected power ( $\approx 350$  W), we determined that 150 W (corresponding to 30  $\mu\text{J}$ ) was absorbed in the MESFET (see figure 4). If the active layer (assumed 0.25- $\mu\text{m}$  thick) with a doping density of  $10^{17} \text{ cm}^{-3}$  were carrying all the current (estimated at 7 A), the peak current density in the active layer would have to exceed  $8 \times 10^6 \text{ A/cm}^2$  for the 200-ns pulse duration. Using a very simple thermal model for the MESFET (Ref. 1), we

would predict that the active layer's temperature rise would be nearly 1000 K. If the temperature had actually reached this level, we would have expected damage from thermal-mode second breakdown (Ref. 2); in this type of instability, the current is concentrated into the hottest regions because of the lower resistance resulting from the thermally increased carrier concentration. Since no damage was observed, the temperature apparently did not reach the  $\approx 750$  K intrinsic temperature. (The intrinsic temperature is defined as that temperature where the number of valence electrons that have sufficient thermal energy to enter the conduction band from the valence band equals the number of conduction band carriers derived from the dopant.) Thus, we believe that a substantial percentage of the energy was absorbed in the substrate.

Infrared and visible light photons are emitted during the intense pulse excitation period; this emission indicates the presence of avalanching. We present preliminary light emission results

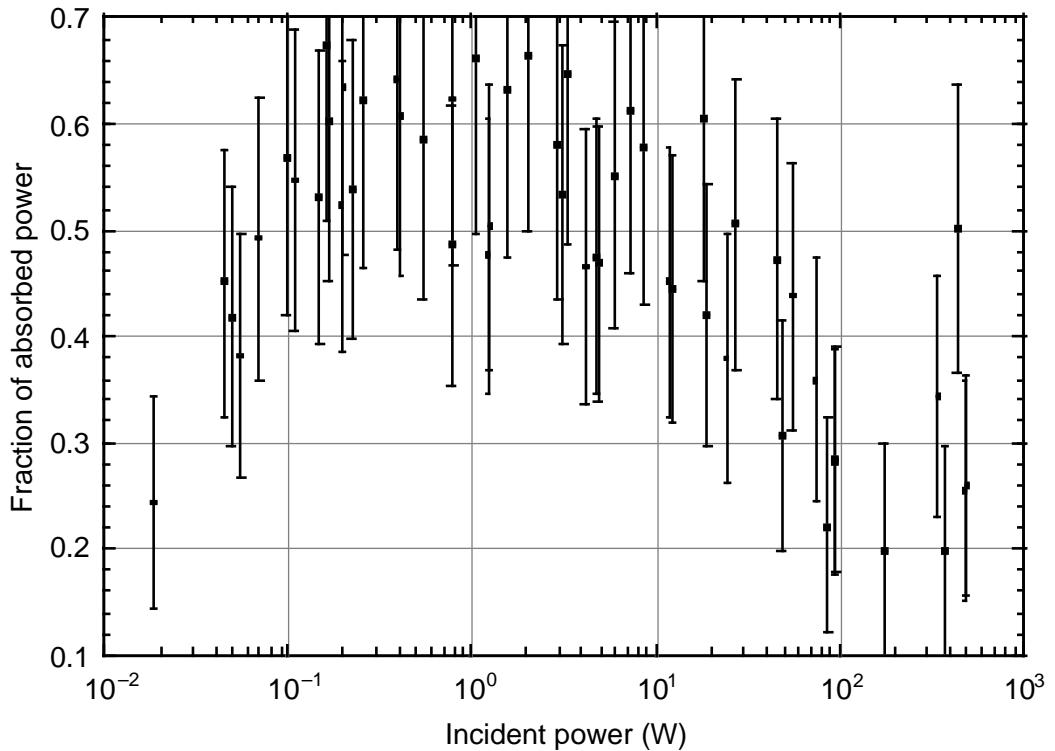


Figure 4. Absorbed power characteristics for MMIC-compatible TPD.

elsewhere (Ref. 1). As a result of our measurements on devices from different foundries, it is clear that different modes of avalanching are occurring, depending on the specifics of the active-layer/substrate interface. Additional work in this topic area is needed, especially because most of the work done in this area involved MESFETs with low-gate-impedance circuits, where excessive gate currents can destroy the gate conductors. Unpublished simulations of the gate current under high-power excitation conditions indicate that total peak gate currents are limited to a few milliamperes, because the external gate circuit resistors are  $1\text{ k}\Omega$  or more.

### DESIGN TECHNIQUE

The design of the TPD is simple. The gate circuit impedance levels should be about 20 times the impedance of the transmission line being protected. With a low-noise FET process, the gate width is selected to pass the current associated with the transmitter pulse at  $I_{dss}$  (zero gate voltage drain-to-source current). If the peak power-handling capability is too low for short pulses, one can increase the gate width by scaling the values in table 1. In most applications, we have observed that the long transmitter pulse lengths are the design driver.

If the insertion loss is too high in the band of interest, the TPD can be tuned with additional reactive components. Because these reactive components are difficult to fabricate at millimeter-wave frequencies, the TPD is not suitable for wideband applications at millimeter-wave frequencies.

### SUMMARY

This TPD design is ideal for phased-array radar applications because it is low-cost, allows minimal spike leakage, and provides adequate isolation. Clearly, Si pin diode TPDs can be designed to equal or outperform this MMIC-compatible TPD, but they require a separate technology, which costs more because of its labor-intensive assembly.

Trantanella et al. (Ref. 3) described a similar power limiter at the 1997 MTT-S Symposium. Their design uses an enhancement-mode MESFET with a series resistor. Two U.S. patents (Nos. 5,157,289 and 5,301,081) also describe circuits similar to that presented here. The circuits that other designers have described are more complex than our circuit, but are expected to provide similar performance.

### ACKNOWLEDGEMENTS

The authors acknowledge major contributions by Thomas Marynowski and Elaine Merenda, and the pioneering work of Carmine Vasile. Without their support this work would have been much more difficult.

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